

Monitoring the Ethernet Interface Status Bits

The Ethernet Interface status bits occupy a single block of either reference memory, or I/O variables. The access type and location of the Ethernet Interface Status bits is specified during configuration of the Ethernet Interface. The Ethernet Status bits are updated in the CPU once each PLC scan by the Ethernet Interface. These bits are generally used to prevent initiation of a COMMREQ function when certain errors occur.

The first 16 bits of the block are the LAN Interface Status (LIS) bits. The next 64 bits are the Channel Status bits (2 for each channel). Unless the “LAN Interface OK” bit is set (Status Bit 16), the other status bits are invalid.

Status Bits	Brief Description
1	Port 1A full duplex
2	Port 1A 100Mbps
3	Port 1B full duplex
4	Port 1B 100 Mbps
5	Reserved
6	Redundant IP address is active (RX7i only)
7-8	Reserved
9	Any Channel Error (error on any channel)
10–12	Reserved
13	LAN OK
14	Resource problem
15	Module Overtemperature (RX3i only)
16	LAN Interface OK
17	Channel 1 Status (SRTP: Data Transfer)
18	Channel 1 Status (SRTP: Channel Error)
...	...
79	Channel 32 Status (SRTP: Data Transfer)
80	Channel 32 Status (SRTP: Channel Error)

LAN Interface Status (LIS) Bits

The LAN Interface Status bits monitor the health of the Ethernet Interface itself.

Bit 1, Port 1a Full Duplex: This bit is set to 1 when Port 1A is set to full duplex. Full-duplex or half-duplex operation is automatically negotiated between the Ethernet Interface and its immediately-connected network device, usually a network hub or switch. If this bit is 0, the port is in half-duplex Ethernet mode. This bit is only valid if bit 13 (LAN OK) is 1.